MICROPROCESSORS AND MICROSYSTEMS

Volume Indices 27 (2003)

Issue 1 pp 1–42
Issue 2 pp 43–100
Issue 3 pp 101–150
Issue 4 pp 151–228
Issues 5–6 pp 229–296
Issue 7 pp 297–352
Issue 8 pp 353–406
Issue 9 pp 407–484
Issue 10 pp 485–540

Article index

Number 1

Telemetry and control system with GSM communications
L. Boquete, I. Bravo, R. Barea, M.A. García 1
PLL based ASIC system for DSP real-time analogue interface
A.E. Mahdi, I.A. Grout 9
Real-time event-handiing and scheduling on a multithreaded Java microcontroller
J. Kreuzinger, U. Brinkschulte, M. Pfeffer, S. Uhrig, Th. Ungerer 19
High performance hardware correlation coefficient assessment using programmable logic for ECG signals
A. Rosado, M. Bataller, J.F. Guerrero, J. Calpe, J.V. Francés, J.R. Magdalena 33

Number 2

Middleware solutions for QoS in distributed multimedia services
P. Bellavista 43
Total quality of service provisioning in middleware and applications
N. Wang, D. C. Schmidt, A. Gokhale, C. D. Gill, B. Natarajan, C. Rodrigues, J. P. Loyall, R. E. Schantz 45
A real time-based architecture for qos multimedia provisioning
D. Cotroneo, G. Iannello, S. Russo, G. Ventre 55
QoS-aware middleware support for collaborative multimedia streaming and caching service
W. J. Jeon, K. Nahrstedt 65
Active middleware for Internet Video on Demand: the QoS-aware routing solution in ubiQoS
P. Bellavista, A. Corradi 73
QoS management for MPEG-4 flows in wireless environment
D. Bruneo, M. Villari, A. Zaia, A. Puliafito 85
MNPA: A basis for privacy-enhanced QoS in mobile networks
B. Askwith, M. Merabti, Q. Shi 93

Number 3

A new scalable broadcast algorithm for multiport meshes with minimum communication steps
A.Y. Al-Dubai, M. Ould-Khaoua 101
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system
C. Tanougast, Y. Berviller, P. Brunet, S. Weber, H. Rabah 115
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model
W. Badawy 131
A scalable multi-porting solution for future wide-issue processors
B. S. Thakar, S. K. Park, G. Lee 141

Number 4

A 12-inch wafer prealigner
H.-S. Lee, J. W. Jeon, J.-W. Kim, S.-J. Jung, J.-E. Byun 151
Establishing timing requirements for control loops in real-time systems
I. Bate, J. McDermid, P. Nightingale 159
An effective out-of-order execution control scheme for an embedded floating point coprocessor
C.-H. Jeong, W.-C. Park, T.-D. Han, S.-B. Yang, M.-K. Lee 171
Disk interface comparison and operating system file-caching investigation
B. Djordjevic, S. Miskovic 181
Processor design based on dataflow concurrency
Sotirios G. Ziavras 199
Implementation of STAP algorithms on IBM SP2 and on ADSP 21062 dual digital signal processor systems
K. Rajan, L.M. Patnaik 221

Numbers 5–6

Editorial
A. K. Somani 229
Flow control scheduling
F. Gramsamer, M. Gusat R. Luijten 233
Stability degree of switches with finite buffers and non-negligible round-trip time
M. Gusat, F. Abel, F. Gramsamer, R. Luijten, C. Minkenberg, M. Verhappen 243
Reconfigurable memory architecture for scalable IP forwarding engines
M. Nourani, M. Akhbarizadeh 253
A software framework for non-repudiation service in electronic commerce based on the Internet
S. Tak, Y. Lee, E. K. Park 265
A design and implementation of active network socket programming
K. L. Eddie Law, R. Leung 277
Intermediate processing protocol for processing within IP-routed networks
S. Pandey, A. Somani A. Tyagi 285

Number 7

Design of SDH STM-1 transmission test set
Y.-G. Show, Y.-C. Chang, Qi-Nan Liao, K.-T. Wu 297
Smoothing voter: a novel voting algorithm for handling multiple errors in fault-tolerant

PII: S0141-9331(03)00151-0

control systems
G. Latif-Shabgahi, S. Bennett, J.M. Bass 303
Asymmetric digital subscriber line access multiplexer—architecture design and implementation
Y.-G. Show, Y.-C. Chang, K.-T. Wu 315
Implementation of model predictive control using real-time multiprocessing computing
G. Hassapis 327
On the suitability of SIMD extensions for neural network simulation
A. Strey 341

Number 8

Past, present and future of data acquisition systems in high energy physics experiments
J. Toledo, F.J. Mora, H. Müller 353
Systolic implementation of 2D block-based Hopfield neural network for efficient pattern association
M.-J. Seow, H. Ngo, V. K. Asari 359
Architecture and instruction set design of an ATM network processor
G. Jones, E. Stipidis 367
A CAD system for the construction and VLSI implementation of Cellular Automata algorithms using VHDL
G.Ch. Sirakoulis, I. Karafyllidis, A. Thanailakis 381
Real-time implementation of an efficient Golay correlator (EGC) applied to ultrasonic sensorial systems
Á. Hernández, J. Ureña, D. Hernanz, J. J. García, M. Mazo, J.-P. Dérutin, J. Serot, S.E. Palazuelos 397

Number 9

Editorial
S. Furber 407
Surfing: a robust form of wave pipelining using self-timed circuit techniques
B. D. Winters, M. R. Greenstreet 409
Balanced self-checking asynchronous logic for smart card applications
S. Moore, R. Anderson, R. Mullins, G. Taylor, J. J. A. Fournier 421
SPA—a secure Amulet core for smartcard applications
L. A. Plana, P. A. Riocreux, W. J. Bainbridge, A. Bardsley, S. Temple, J. D. Garside, Z. C. Yu 431
Clock synchronization through handshake signalling
J. Kessels, A. Peeters, P. Wielage, S.-J. Kim 447
Adding synchronous and LSSD modes to asynchronous circuits
K. van Berkel, A. Peeters, F. te Beest 461
On-chip structures for timing measurement and test
D. J. Kinniment, O. V. Maevsky, A. Bystrov, G. Russell, A. V. Yakovlev 473

Number 10

An asynchronous copy-back cache architecture
D. Hormdee, J. D. Garside, S. B. Furber 485
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor
R. Subramaniam, R. Sharadh, K. M. M. Prabhu 501
The fractional Fourier transform: theory, implementation and error analysis
V. Ashok Narayanan, K. M. M. Prabhu 511
Generating test sequences using symbolic execution for event-driven real-time systems
N. H. Lee, S. D. Cha 523

Author Index

Abel, F. 243
Akhbarizadeh, M. 253
Al-Dubai, A. Y. 101
Anderson, R. 421
Asari, V. K. 359
Ashok Narayanan, V. 511
Askwith, B. 93

Badawy, W. 131
Bainbridge, W. J. 431
Bardsley, A. 431
Barea, R. 1
Bass, J. M. 303
Bataller, M. 33
Bate, I. 159
Beest, F. te 461
Bellavista, P. 43, 73
Bennett, S. 303
Berkel, K. van. 461
Berviller, Y. 115
Boquete, L. 1
Bravo, I. 1
Brinkschulte, U. 19
Bruneo, D. 85
Brunet, P. 115
Bystrov, A. 473
Byun, J.-E. 151

Calpe, J. 33
Cha, S. D. 523
Chang, Y.-C. 297, 315
Corradi, A. 73
Cotroneo, D. 55

Dérutin, J.-P. 397
Djordjevic, B. 181

Fournier, J. J. A. 421
Francés, J. V. 33
Furber, S. B. 485
Furber, S. 407

García, M. A. 1
Garside, J. D. 431, 485
Gill, C. D. 45
Gokhale, A. 45
Gramsamer, F. 233, 243
Greenstreet, M. R. 409
Grout, I. A. 9
Guerrero, J. F. 33
Gusat, M. 233, 243

Han, T.-D. 171
Hassapis, G. 327
Hernanz, D. 397
Hernández, Á. 397
Hormdee, D. 485

Iannello, G. 55

Jeon, J. W. 151
Jeon, W. J. 65
Jeong, C.-H. 171
Jesús Garcia, J. 397
Jones, G. 367
Jung, S.-J. 151

Karafyllidis, I. 381
Kessels, J. 447
Kim, J.-W. 151
Kim, S. J. 447
Kinniment, D. J. 473
Kreuzinger, J. 19
Kreuzinger, J. 19

Latif-Shabgahi, G. 303
Law, K. L. E. 277
Lee, G. 141
Lee, H.-S. 151
Lee, M.-K. 171
Lee, N. H. 523
Lee, Y. 265
Leung, R. 277
Liao, Q.-N. 297
Loyall, J. P. 45
Luijten, R. 233, 243

Maevsky, O. V. 473
Magdalena, J. R. 33
Mahdi, A. E. 9
Mazo, M. 397
McDermid, J. 159
Merabti, M. 93
Minkenberg, C. 243
Miskovic, S. 181
Moore, S. 421
Mora, F. J. 353
Müller, H. 353
Mullins, R. 421

Nahrstedt, K. 65
Natarajan, B. 45
Ngo, H. 359
Nightingale, P. 159
Nourani, M. 253

Ould-Khaoua, M. 101

Palazuelos, S. E. 397
Pandey, S. 285
Park, E. K. 265
Park, S. K. 141
Park, W.-C. 171
Patnaik, L. M. 221
Peeters, A. 447, 461
Pfeffer, M. 19
Plana, L. A. 431

Prabhu, K. M. M. 501, 511
Puliafito, A. 85

Rabah, H. 115
Rajan, K. 221
Rodrigues, C. 45
Roicreux, P. A. 431
Rosado, A. 33
Russell, G. 473
Russo, S. 55

Schantz, R. E. 45
Schmidt, D. C. 45
Seow, M.-J. 359
Serot, J. 397
Sharadh, R. 501
Shi, Q. 93
Show, Y.-G. 297, 315
Sirakoulis, G.Ch. 381
Somani, A. 285
Stipidis, E. 367
Strey, A. 341
Subramaniam, R. 501

Tak, S. 265
Tanougast, C. 115
Taylor, G. 421
Temple, S. 431
Thakar, B. S. 141
Thanailakis, A. 381
Toledo, J. 353
Tyagi, A. 285

Uhrig, S. 19
Uhrig, S. 19
Ungerer, Th. 19
Ureña, J. 397

Ventre, G. 55
Verhappen, M. 243
Villari, M. 85

Wang, N. 45
Weber, S. 115
Wielage, P. 447
Winters, B. D. 409
Wu, K.-T. 297, 315

Yakovlev, A. V. 473
Yang, S.-B. 171
Yu, Z. C. 431

Ziavras, S.G. 199

Keyword Index

Active applications
A design and implementation of active network socket programming 277
Active network socket programming
A design and implementation of active network socket programming 277
Active networking
Intermediate processing protocol for processing within IP-routed networks 285
Active networks
A design and implementation of active network socket programming 277
Active Services
Active middleware for Internet Video on Demand: the QoS-aware routing solution in ubiQoS 73
Admissible
Stability degree of switches with finite buffers and non-negligible round-trip time 243
ADSP-2192 processor
The fractional Fourier transform: theory, implementation and error analysis 511
ADSP-2192
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Amulet processor
SPA—a secure Amulet core for smartcard applications 431
Analogue interface
PLL based ASIC system for DSP real-time analogue interface 9
Application programming interface
A design and implementation of active network socket programming 277
Application specific integrated circuit
PLL based ASIC system for DSP real-time analogue interface 9
Asymmetric digital subscriber line
Asymmetric digital subscriber line access multiplexer—architecture design and implementation 315
Asynchronous circuits
Surfing: a robust form of wave pipelining using self-timed circuit techniques 409
Adding synchronous and LSSD modes to asynchronous circuits 461
Asynchronous crossbar/bus
Clock synchronization through handshake signalling 447
Asynchronous design
An asynchronous copy-back cache architecture 485
Asynchronous logic
Balanced self-checking asynchronous logic for smart card applications 421
Asynchronous processor
SPA—a secure Amulet core for smartcard applications 431
Asynchronous synthesis system
SPA—a secure Amulet core for smartcard applications 431
Asynchronous transfer mode
Architecture and instruction set design of an ATM network processor 367
ATA
Disk interface comparison and operating system file-caching investigation 181
ATM
Asymmetric digital subscriber line access multiplexer—architecture design and implementation 315
Automatic VLSI implementation
A CAD system for the construction and VLSI implementation of Cellular Automata algorithms using VHDL 381
Availability
Smoothing voter: a novel voting algorithm for handling multiple errors in fault-tolerant control systems 303

Backpressure
Stability degree of switches with finite buffers and non-negligible round-trip time 243
Bit Error Rate Tester
Design of SDH STM-1 transmission test set 297
Buffered packet switch
Flow control scheduling 233
Bus architecture
Past, present and future of data acquisition systems in high energy physics experiments 353

Cache architecture
An asynchronous copy-back cache architecture 485
Caching
QoS-aware middleware support for collaborative multimedia streaming and caching service 65
Cellular Automata
A CAD system for the construction and VLSI implementation of Cellular Automata algorithms using VHDL 381
Collective communication
A new scalable broadcast algorithm for multiport meshes with minimum communication steps 101
Comparative analysis
Processor design based on dataflow concurrency 199
Computational complexity and computational speed
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Concurrent operations
Processor design based on dataflow concurrency 199
Control
Telemetry and control system with GSM communications 1
Control systems
Establishing timing requirements for control loops in real-time systems 159
Coprocessor
An effective out-of-order execution control scheme for an embedded floating point coprocessor 171
Copy-back cache
An asynchronous copy-back cache architecture 485
CORBA Component Model
Total quality of service provisioning in middleware and applications 45
Correlation
High performance hardware correlation coefficient assessment using programmable logic for ECG signals 33
CPU
A real time-based architecture for qos multimedia provisioning 55
credit flow control
Flow control scheduling 233

Data acquisition
Past, present and future of data acquisition systems in high energy physics experiments 353
Data-driven (dataflow) model of computation
Processor design based on dataflow concurrency 199
Data-parallel processing
On the suitability of SIMD extensions for

neural network simulation 341
Design implementation
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115
Differential power analysis
Balanced self-checking asynchronous logic for smart card applications 421
Digital signal processor
PLL based ASIC system for DSP real-time analogue interface 9
Digital subscriber line access multiplexer
Asymmetric digital subscriber line access multiplexer—architecture design and implementation 315
Discrete Fourier transform
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Discrete fractional Fourier transform
The fractional Fourier transform: theory, implementation and error analysis 511
Disk-interfaces
Disk interface comparison and operating system file-caching investigation 181
Distributed computing
Intermediate processing protocol for processing within IP-routed networks 285
Distributed CPU
Processor design based on dataflow concurrency 199
Domino logic
Surfing: a robust form of wave pipelining using self-timed circuit techniques 409
DTV
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131
Dual tone multi-frequency
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Dynamical systems
Surfing: a robust form of wave pipelining using self-timed circuit techniques 409
Dynamically reconfigurable systems
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115

Electrocardiogram
High performance hardware correlation coefficient assessment using programmable logic for ECG signals 33
Telemetry and control system with GSM communications 1
Electromagnetic emissions analysis
Balanced self-checking asynchronous logic for smart card applications 421
Electronic commerce
A software framework for non-repudiation service in electronic commerce based on the Internet 265
Embedded system
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115
An effective out-of-order execution control scheme for an embedded floating point coprocessor 171
Embedded systems
Implementation of model predictive control using real-time multiprocessing computing 327
Error analysis
The fractional Fourier transform: theory, implementation and error analysis 511
Execution environments
A design and implementation of active network socket programming 277

Fast Fourier transform
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Fault-tolerance
Smoothing voter: a novel voting algorithm for handling multiple errors in fault-tolerant control systems 303
Field programmable gate arrays
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115
File caching
Disk interface comparison and operating system file-caching investigation 181
File system
Disk interface comparison and operating system file-caching investigation 181
Fixed-point processor
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Floating-point unit
An effective out-of-order execution control scheme for an embedded floating point coprocessor 171
Flow control scheduling
Flow control scheduling 233
Forwarding engine
Reconfigurable memory architecture for scalable IP forwarding engines 253
Fourier transform
The fractional Fourier transform: theory, implementation and error analysis 511
FPGA
High performance hardware correlation coefficient assessment using programmable logic for ECG signals 33
Design of SDH STM-1 transmission test set 297
Real-time implementation of an efficient Golay correlator (EGC) applied to ultrasonic sensorial systems 397

GALS systems
Clock synchronization through handshake signalling 447
Golay sequences
Real-time implementation of an efficient Golay correlator (EGC) applied to ultrasonic sensorial systems 397
Grid computing
QoS management for MPEG-4 flows in wireless environment 85

2D hierarchical mesh-based video object model
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131
High-level synthesis
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115
Hopfield network
Systolic implementation of 2D block-based Hopfield neural network for efficient pattern association 359

Image processing
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115
Implementation
The fractional Fourier transform: theory, implementation and error analysis 511
12-inch wafer
A 12-inch wafer prealigner 151
Industrial control
Implementation of model predictive control using real-time multiprocessing computing 327
Interconnection networks
A new scalable broadcast algorithm for multiport meshes with minimum communication steps 101
Intermediate processing
Intermediate processing protocol for processing within IP-routed networks 285
Intermediate processing protocol
Intermediate processing protocol for processing within IP-routed networks 285
Internet protocol
Reconfigurable memory architecture for scalable IP forwarding engines 253
IP address
Reconfigurable memory architecture for scalable IP forwarding engines 253

Java processor
Real-time event-handling and scheduling on a multithreaded Java microcontroller 19

Level-sensitive scan design
Adding synchronous and LSSD modes to asynchronous circuits 461
Longest prefix matching
Reconfigurable memory architecture for scalable IP forwarding engines 253

Machine-to-machine
Telemetry and control system with GSM communications 1
Microcontroller
Telemetry and control system with GSM communications 1
Microprocessors
On the suitability of SIMD extensions for neural network simulation 341
Middleware
Total quality of service provisioning in middleware and applications 45
QoS-aware middleware support for collaborative multimedia streaming and

caching service 65
Active middleware for Internet Video on Demand: the QoS-aware routing solution in ubiQoS 73
Mobile agents
Active middleware for Internet Video on Demand: the QoS-aware routing solution in ubiQoS 73
QoS management for MPEG-4 flows in wireless environment 85
Mobile networks
MNPA: A basis for privacy-enhanced QoS in mobile networks 93
Mobile telephony
Telemetry and control system with GSM communications 1
Modechart
Generating test sequences using symbolic execution for event-driven real-time systems 523
Model based development
Establishing timing requirements for control loops in real-time systems 159
Modelling
A CAD system for the construction and VLSI implementation of Cellular Automata algorithms using VHDL 381
Modular architecture
Systolic implementation of 2D block-based Hopfield neural network for efficient pattern association 359
Motion Estimation
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131
MPEG
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131
MPEG-4
QoS management for MPEG-4 flows in wireless environment 85
Multi-emission
Real-time implementation of an efficient Golay correlator (EGC) applied to ultrasonic sensorial systems 397
Multimedia
QoS-aware middleware support for collaborative multimedia streaming and caching service 65
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131
Multiplexer
Asymmetric digital subscriber line access multiplexer—architecture design and implementation 315
Multiprocessing
Implementation of model predictive control using real-time multiprocessing computing 327
Multiprocessor systems
Past, present and future of data acquisition systems in high energy physics experiments 353
Multithreaded microcontroller
Real-time event-handling and scheduling on a multithreaded Java microcontroller 19
Multithreaded processor
Real-time event-handling and scheduling on a multithreaded Java microcontroller 19
Network processor architecture
Architecture and instruction set design of an ATM network processor 367
Neural networks
On the suitability of SIMD extensions for neural network simulation 341
Non-repudiation
A software framework for non-repudiation service in electronic commerce based on the Internet 265
Non-uniform discrete Fourier transform
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501

On-chip test
On-chip structures for timing measurement and test 473
Optical character recognition
A 12-inch wafer prealigner 151
Out-of-order execution
An effective out-of-order execution control scheme for an embedded floating point coprocessor 171

Parallel algorithms
Implementation of model predictive control using real-time multiprocessing computing 327
Partitioned lookup table
Reconfigurable memory architecture for scalable IP forwarding engines 253
Pattern association
Systolic implementation of 2D block-based Hopfield neural network for efficient pattern association 359
Pausible clocks
Clock synchronization through handshake signalling 447
Performance analysis
A new scalable broadcast algorithm for multiport meshes with minimum communication steps 101
Prealigner
A 12-inch wafer prealigner 151
Prefix matching
Reconfigurable memory architecture for scalable IP forwarding engines 253
Privacy
MNPA: A basis for privacy-enhanced QoS in mobile networks 93
Processor design
Processor design based on dataflow concurrency 199
Processor/memory architectures
Clock synchronization through handshake signalling 447
Programmable logic
High performance hardware correlation coefficient assessment using programmable logic for ECG signals 33

QoS
A real time-based architecture for qos multimedia provisioning 55
QoS management
QoS management for MPEG-4 flows in wireless environment 85
Quality of service adaptation
Total quality of service provisioning in middleware and applications 45
Quality of service provisioning
Total quality of service provisioning in middleware and applications 45
Quality of service
QoS-aware middleware support for collaborative multimedia streaming and caching service 65
Active middleware for Internet Video on Demand: the QoS-aware routing solution in ubiQoS 73
MNPA: A basis for privacy-enhanced QoS in mobile networks 93
Rate monotonic
A real time-based architecture for qos multimedia provisioning 55
Real-time event handling
Real-time event-handling and scheduling on a multithreaded Java microcontroller 19
Real-time processing
PLL based ASIC system for DSP real-time analogue interface 9
Real-time scheduling
Real-time event-handling and scheduling on a multithreaded Java microcontroller 19
Real-time system testing
Generating test sequences using symbolic execution for event-driven real-time systems 523
Real-time systems
Establishing timing requirements for control loops in real-time systems 159
Implementation of model predictive control using real-time multiprocessing computing 327
Reconfigurable memory architecture
Reconfigurable memory architecture for scalable IP forwarding engines 253
Ring oscillator
Clock synchronization through handshake signalling 447
Round-trip time
Flow control scheduling 233
Route lookup table
Reconfigurable memory architecture for scalable IP forwarding engines 253
Router
Reconfigurable memory architecture for scalable IP forwarding engines 253
RTT
Stability degree of switches with finite buffers and non-negligible round-trip time 243
Run-time reconfiguration
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115

Safety
Smoothing voter: a novel voting algorithm for handling multiple errors in fault-tolerant control systems 303
Safety-critical system
Smoothing voter: a novel voting algorithm for handling multiple errors in fault-tolerant control systems 303
Scheduling
Establishing timing requirements for control loops in real-time systems 159
Security
MNPA: A basis for privacy-enhanced QoS in mobile networks 93

A software framework for non-repudiation service in electronic commerce based on the Internet 265
Balanced self-checking asynchronous logic for smart card applications 421
Self-timed system
SPA—a secure Amulet core for smartcard applications 431
Set-up time
On-chip structures for timing measurement and test 473
Shift register latches
Adding synchronous and LSSD modes to asynchronous circuits 461
SIMD extensions
On the suitability of SIMD extensions for neural network simulation 341
Simulation
A CAD system for the construction and VLSI implementation of Cellular Automata algorithms using VHDL 381
Small computer system interface
Disk interface comparison and operating system file-caching investigation 181
Smart card
Balanced self-checking asynchronous logic for smart card applications 421
Smartcard security
SPA—a secure Amulet core for smartcard applications 431
Software framework
A software framework for non-repudiation service in electronic commerce based on the Internet 265
Stability
Stability degree of switches with finite buffers and non-negligible round-trip time 243
Streaming
QoS-aware middleware support for collaborative multimedia streaming and caching service 65
Sub-band non-uniform discrete Fourier transform
Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor 501
Switching
Stability degree of switches with finite buffers and non-negligible round-trip time 243
Symbolic execution
Generating test sequences using symbolic execution for event-driven real-time systems 523
Synchronous Digital Hierarchy
Design of SDH STM-1 transmission test set 297
System on Chip
High performance hardware correlation coefficient assessment using programmable logic for ECG signals 33
Systolic implementation
Systolic implementation of 2D block-based Hopfield neural network for efficient pattern association 359

Telemetry
Telemetry and control system with GSM communications 1
Temporal partitioning
Temporal partitioning methodology optimizing FPGA resources for dynamically reconfigurable embedded real-time system 115
Test set
Design of SDH STM-1 transmission test set 297
Test-pattern generation
Adding synchronous and LSSD modes to asynchronous circuits 461
Time measurement
On-chip structures for timing measurement and test 473
Timing
Surfing: a robust form of wave pipelining using self-timed circuit techniques 409
Timing margins
On-chip structures for timing measurement and test 473
Ultrasonic system
Real-time implementation of an efficient Golay correlator (EGC) applied to ultrasonic sensorial systems 397

Velocity command
A 12-inch wafer prealigner 151
VHDL
A CAD system for the construction and VLSI implementation of Cellular Automata algorithms using VHDL 381
Video
Telemetry and control system with GSM communications 1
Video object plane
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131
Video on Demand
Active middleware for Internet Video on Demand: the QoS-aware routing solution in ubiQoS 73
Virtual output queueing
Flow control scheduling 233
VLSI architecture
A VLSI architecture for video object motion estimation using a 2D hierarchical mesh model 131

Wave-pipelining
Surfing: a robust form of wave pipelining using self-timed circuit techniques 409
Wireless systems
QoS management for MPEG-4 flows in wireless environment 85
Wormhole routing
A new scalable broadcast algorithm for multiport meshes with minimum communication steps 101